Implementation of Power Management in High Speed Electronic Devices

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Abstract

This paper describes techniques to manage the power consumption of high-speed programmable logic devices (PLDs). Power consumption has become an increasingly important issue to system designers as the speed (and thus power consumption) of programmable logic devices has increased. To address power consumption concerns, design engineers need to accurately predict the power conumption of a design before the design is implemented on the board. When power consumption is too high, there are many design approaches and device features that can reduce the ultimate power consumption of the design.

Keywords : Prgrammable Logic Devices, Design Approach, Power consumption and Integrated Circuits.

1. Introduction

Since power is a direct function of operating frequency, power consumption has become a greater issue as system performance has increased.[1][2][3]. Initially the concern of only the few designers working on portable equipment, power consumption is now important to a growing number of design engineers working on everything from PC add-on cards to telecom equipment. In logic ICs, power consumption is a direct function of factors such as gate count, operating frequency, and pin count.[4][5]. As these fundamental metrics of the logic semiconductor industry continue to grow, power consumption will grow as well.Fortunately for power-conscious designers, several PLDs offer options to reduce power consumption.[7][8] These features, along with an eventual migration to 3.3-volt devices will keep power consumption issues manageable.[9]

2. The Components of Power Consumption

The total power consumed by a PLD is made up of three major components: standby, internal, and external. An equation for total power (P_{TOTAL}), shown below, reflects these three contributions:

$P_{TOTAL} = P_{STANDBY} + P_{INTERNAL} + P_{EXTERNAL}$

Where: $P_{STANDBY}$ is the standby power consumed by the powered device when no inputs are toggling.

$P_{INTERNAL}$ is the power associated with the active internal circuitry and is a function of the clock frequency.

$P_{EXTERNAL}$ is the power associated with driving the output signals and is a function of the number of outputs, the output load, and the output toggle frequency.

Figure 1 shows the power consumption of a 2,500-gate PLD broken down into $P_{STANDBY}$, $P_{INTERNAL}$, and $P_{EXTERNAL}$. As indicated in the figure, power consumption is strong function of frequency, and the internal and external power consumption are large contributors at the frequencies typically found in today's systems. The standby power is a significant factor only at low frequencies.[9][10].

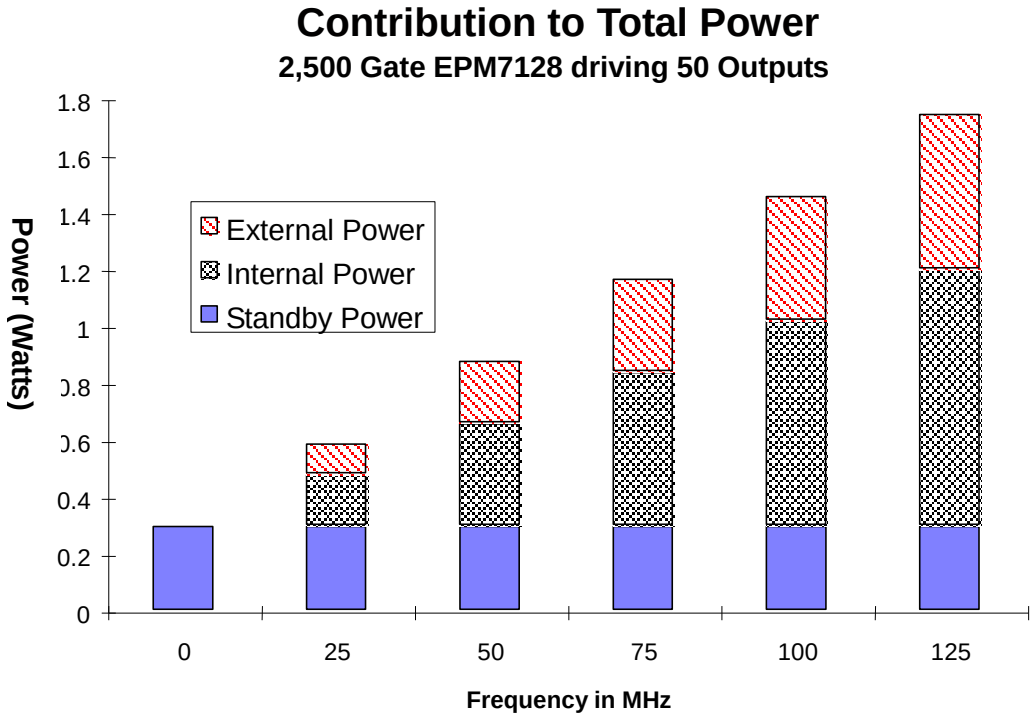

Figure 1. Contributing factors to Power Consumption.[10]

This graph shows the three contributing factors to the total power consumption. The total power is dominated by the frequency dependent internal and external power.

3. Estimating Power Consumption

The total power consumption of a device can be estimated from the power consumption contribution of each of the three factors.

3.1 Standby Power

The standby power consumption of a device depends primarily on the type of logic element used. Programmable logic that use look-up tables (LUTs) or multiplexors as the basic logic element tend to have a low standby power, typically less than 500 uW. This low standby power is primarily due to the leakage current present in all CMOS logic devices. Examples of products in this class include Altera FLEX 8000 devices and FLEX 10K devices, Xilinx FPGAs, and Actel FPGAs.

On the other hand, devices that use product terms as the basic logic cell typically have a standby power between 50 and 500 mW. In these devices the active pull-down transistors on the product terms are the primary source of standby power. This passive pull-up, active pull-down structure means that product terms are consuming power even in a static state. There are a few exceptions to this rule (as indicated in the Managing Power In Programmable Logic section).

3.2 Internal Power

The internal power consumption of programmable logic devices is due to the switching of signals within the device. Each time a signal is raised and lowered, current flows into and out of the device, thereby increasing the power consumption.

To help engineers estimate the internal power consumption of their designs, most PLD vendors publish equations or graphs that estimate the internal current consumption of a device as a function of the operating frequency and the resource utilization of the device.

For example, the following equation is used to estimate the internal current consumption of Altera's FLEX 8000 devices:

$$I_{INTERNAL} = KFNp.$$

In this equation, K is a constant equal to 75 uA/MHz/LE, meaning that each logic element (LE) consumes 75 uA for each full cycle transition. F is the master system frequency, N is the number of LEs, and p is the percentage of LEs that toggle on each clock edge. A conservative estimate for p is 12.5% (0.125).

Using this equation reveals that a 2,500-gate design (200 logic elements) running at 50 MHz will consume approximately 93 mA, or 468 mW, due to internal circuitry.

3.3 External Power

The external power consumed is dependent on only two main factors: the output load and the output toggle frequency. Because both of these factors are independent of the device type, the external power consumption is dependent entirely on the design, not the device.

A good approach to estimating external power is to use the following equation:

$$P_{EXTERNAL} = 1/2 \sum C_n F_n V_n^2.$$

In this equation C_n is the capacitive load of output pin n, F_n is the toggle frequency of pin n, and V_n^2 is the voltage swing of pin n. Assuming that C, F, and V is the same for each pin, the equation simplifies to:

$$P_{EXTERNAL} = 1/2\ ACpF\ V^2,$$

where A is the number of outputs, C is the average load, F is the system frequency, and V is the average voltage swing. The factor p is the estimated number of clock cycles that an output pin toggles. A conservative estimate for p is 20% (0.2).

Currently, most PLDs drive TTL output voltages with an NMOS pull-up transistor. Using an NMOS instead of PMOS transistor makes the voltage swing approximately 3.8 volts, rather than the full 5.0-volt rail. Devices with CMOS output drive options or internal pull-up resistors have a higher output voltage and significantly higher power consumption.

Output switching contributes significantly to the power consumption of an application, regardless of the device chosen. For example, a 50-MHz application with 50 output pins driving 35-pF loads would consume approximately 126 mW of power, as shown in the following equation:

$$P_{EXTERNAL} = 1/2\ (50\ pins)(35\ pF/pin)\ (20\%)(50\ MHz)(3.8\ V)^2 = 126\ mW.$$

4. Managing Power in Programmable Logic

There are several approaches to managing power consumption in programmable logic. The easiest approach is to take advantage of the power consumption features offered by many programmable logic devices. Switching to 3.3-volt PLDs is another option. Programmable logic devices that run at 3.3 volts are now available from a few vendors, with more to come in the near future. In the mean time, 3.3V/5.0V hybrid devices are the perfect choice for designers who need to use components that require both power supply standards.

Many of the programmable logic devices available today have features that can be used to manage power consumption, including automatic power-down, programmable speed/power control, and pin-controlled power down. Different applications benefit from different approaches to power consumption management. The following descriptions of the different

approaches and their impact on power consumption can help you choose the features that are appropriate for your application.

4.1 Automatic Power-Down

To reduce standby power consumption, some EPROM-based PLDs offer an automatic power-down feature. These devices contain internal power-down circuitry that continually monitors the inputs and internal signals of a device, and powers down the internal EPROM array after approximately 100 ns of inactivity. When an input changes, the EPROM array is then powered up and the device behaves as normal. For example, Altera Classic devices offer a power-down feature (called the "zero-power mode") enabled and disabled. The zero-power mode eliminates the power consumed by the product-terms, reducing the standby power consumption to that consumed by CMOS leakage current.

4.2 Programmable Speed/Power Control

Some programmable devices allow the designer to trade off between speed and power. Since many applications have only a few truly speed-critical paths, a designer can choose to run parts of the design at high speed while the rest of the design runs at low power. For designers that require high speed in at least some portion of their design, this feature may provide the most effective means of managing power consumption.

For example, with MAX 7000 and MAX 9000 devices, each macrocell can be programmed by the designer to operate in the turbo mode or low-power mode. The turbo mode offers higher performance with normal power consumption, while the low-power mode offers reduced power consumption with lower performance. The low-power mode reduces the macrocell's power consumption by 50% while increasing the delay by 7-15 ns, depending on the speed grade.

Figure 2 shows the power consumed by an Altera MAX 7000 device under two conditions: one in which the turbo mode is turned on for all macrocells in the device, and one in which the low-power mode options are turned on for all the macrocells in the device. The actual power consumed by a design would lie between the two lines depending on how many macrocells are set in each mode.

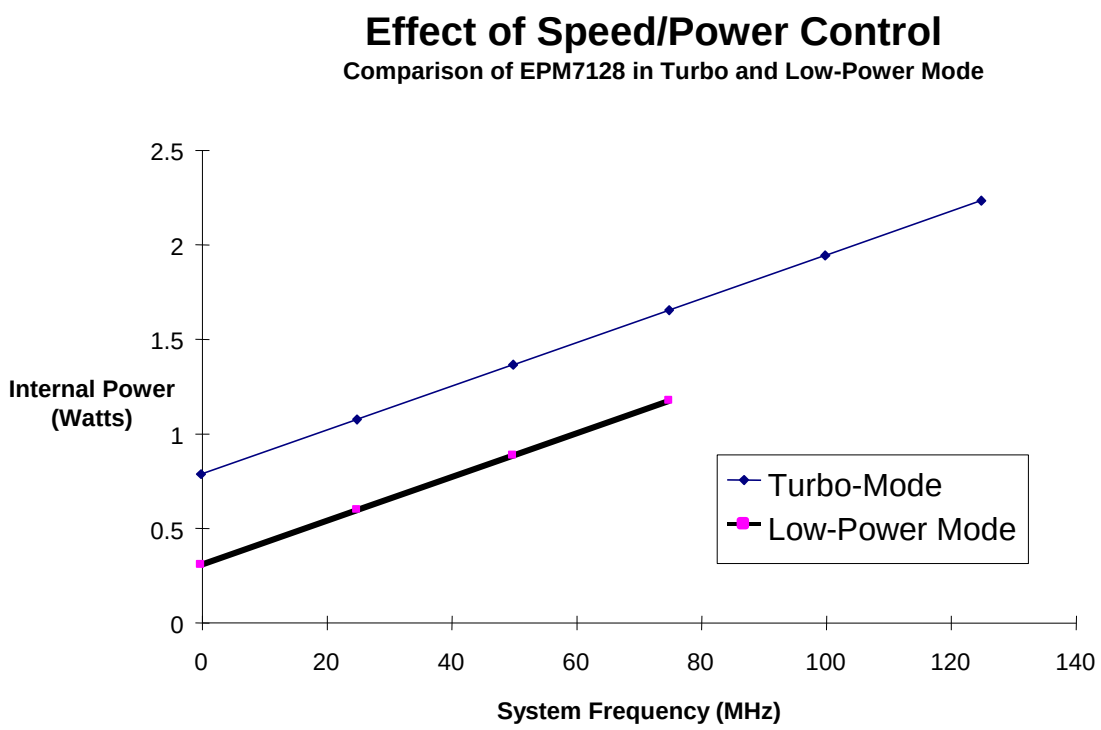

Figure 2. Programmable Speed/Power Control

The EPM7128E offers speed/power control on a macrocell-by-macrocell basis. This graph shows the power consumption with all the macrocells in either the turbo or low-power mode.

4.3 Pin-Controlled Power Down

Some programmable logic devices offer a power-down mode that is controlled by an external pin. This method of power management allows the designer to power-down portions of a board that are not in use. A typical example is a laptop motherboard that powers down the disk drive and associated logic when the drive is not in use.

When the device is powered down, the outputs still drive valid signals and the internal values of all registers remain valid. When the power-down pin is deactivated, the device responds to new inputs within a set amount of time (700 ns, in the case of the EPM7032V).

4.4 3.3-volt Devices

One of the most effective approaches to reducing power consumption is to move to a 3.3-volt device. Reducing the voltage has a square law effect on the power consumption. As shown in the internal power consumption equation, a reduction in voltage from 5.0 to 3.3 volts can reduce the internal power consumption by up to 57%.

Figure 3 shows the internal power consumption of two Altera FLEX 8000 devices. One device is the 5.0-volt EPF8282A and the other device is the 3.3-volt version known as the EPF8282V. The same application is running in both devices at the same speed, using 90% of device resources. In the case of the 3.3-volt device, the power reduction is close to 50%.

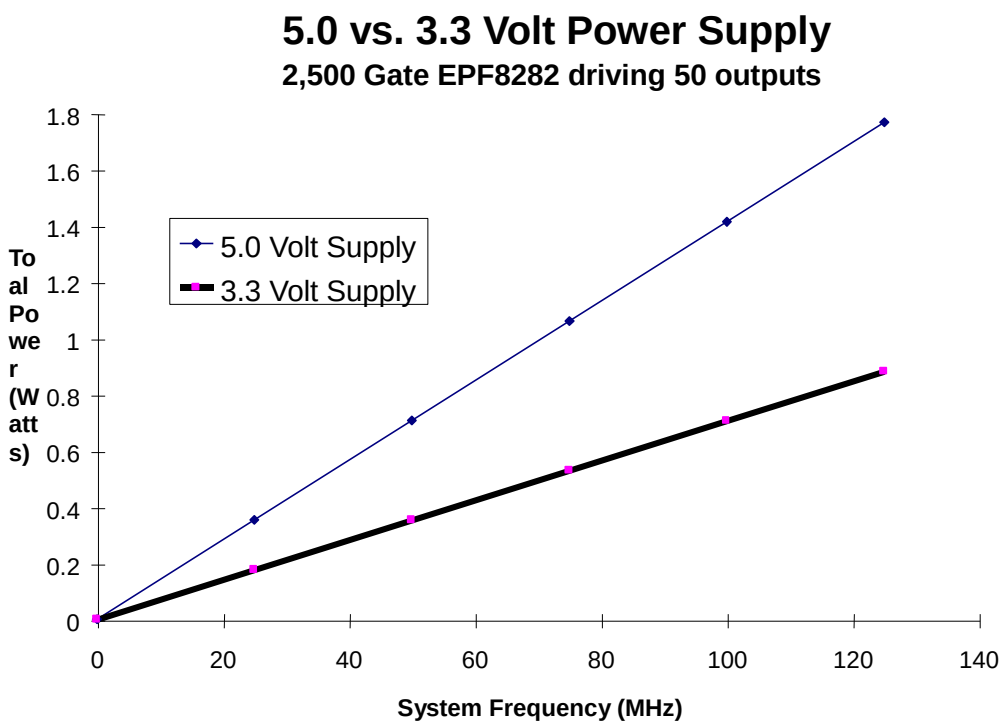

Figure 3. 3.3 Volt Power Reduction

Switching to 3.3 volts is the most effective means of reducing power consumption. This graph compares the power consumed by the 5.0-volt EPF8282A and the 3.3-volt EPF8282V.

4.5 3.3-Volt / 5.0-Volt Hybrid Devices

To help accelerate the inevitable transition from 5.0-volt to 3.3-volt devices, some programmable logic vendors offer devices that can be programmed to drive either 3.3-volt or 5.0-volt outputs and can accept either 5.0-volt or 3.3-volt inputs. By allowing engineers to bridge the transition between 5.0-volt and 3.3-volt technology, these devices enable overall power reduction by allowing lower power-consuming 3.3-volt devices to be used with 5.0-volt devices. Without these hybrid "bridge" devices, designers would have to wait until every device used in the design was available in a 3.3-volt version.

The greatest reduction in power consumption results from a transition to 3.3-volts, and using these hybrid devices eases and facilitates the transition.

Conclusion

Power consumption is a critical issue in many designs today. With gate counts, operating frequency, and pin counts increasing, power consumption must also increase if it is not offest by other factors. The most promising relief from increasing power consumption is the migration from 5.0-volt to 3.3-volt power supplies. This migration alone can cut power consumption by as much as 60%. In addition, several programmable logic devices have many unique approaches to reducing power consumption within the device. From programmable speed/power control to automatic power-down, each approach offers a unique set of benefits and tradeoffs. Designers must understand the options offered by the each family of devices in order to make the right choice for their applications.

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